ICM107B Mega pixel Color CMOS image sensor

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Features

- 1 mega pixels (1152x864) format, used with 1/2" optical system
- Support sub-sampling at quarter (1/4) mega pixel resolution for higher video frame rate
- Progressive readout
- Output data format: 10-bit raw data
- Input interface: SIF
- Electronic exposure control
- On-chip 11-bit ADC
- On-chip PLL
- Correlated double sampling
- Video mode and DSC mode
- Dead pixel removal
- Flash control
- Power down mode
- Automatic optical black compensation
- Horizontal and veritcal images
- Single 3.3V power supply

General Description

ICM-107B is a single-chip digital color-imaging device. It incorporates a 1152x864 sensor array capable of operating at up to 30 frames per second and sub-sampled quarter mega pixel resolution, operating at higher frame rate in progressive manner. Each pixel is covered by a color filter, which formed a so-called Bayer pattern. Correlated double sampling is performed by the internal ADC and timing circuitry. The gains for raw data can be adjusted separately for the 4 Bayer pattern pixels. The output format is 10-bit raw data that can be fed to other DSP, color processing, or compression chips.

Applications

- Digital camcorder
- Digital still camera
- Video phone
- Video conferencing
- Video mail
- Video cellular phone
- PC camera
- Security system
- Visual toy
- Industrial image capture/analysis
- Environment monitor system

Key Parameters

- Number of pixels: 1152x864
- Number of physical pixels: 1,015,588, (1162x874)

- Frame rate: 30/15/10/5/4/3/2/1 fps
- Sub-sampling quarter mega pixel for higher frame rate
- Pixel size: 6 µm x 6 µm
- Sensor area: 6.9 mm x 5.18 mm
- Input clock: 6 MHz crystal, or external clock source of 6, 12, 24, 48, or 96 MHz through PLL or bypass PLL
- Main clock frequency: 48 MHz; on-chip 11 bit ADC clock: 96MHz (2x of main clock frequency), for 30 fps operation.
- Mode exposure time: 31.25 µs (@ 30 fps, 1 line). Maximum exposure time ~ 60 s @ X1 mode (1 fps), 65535 lines
- RGB gain: 1/256 to 64 for individual Bayer pattern pixels depending on register setting.
- Sensitivity: 1.0 V/lux-sec (5200 K light source, 650 nm IR cutoff filter)
- Quantum Efficiency: 38 % (555 nm)
- Dynamic Range: 55 dB (relative to noise floor = temporal noise + quantization noise); 45 dB (relative to total noise)
- Fill Factor: 28%
- S/N Ratio(temporal noise): 45 dB @ 75% full signal level
- S/N Ratio(total noise): 40 dB @ 75% full signal level
- Sensitive to infrared illumination source
- Power supply: 3.3V
- Power requirement: <100mA (@30fps) and <60mA (@15fps)
- Standby mode power: < 50uA
- Package: Plastic LCC48

1. Preliminary Pin Assignment

Pin #	Name	Class*	Function
14	CLKSEL	D, I, N	Clock source selection 0: clocks pass PLL, use XIN (pin 12) 1: bypass PLL, use CLKIN (pin 11)
11	CLKIN	D, I, N	External clock source; bypass PLL
12	XIN	A, I	Crystal oscillator in, or external clock in; if external clocks used, leave Xout (pin 13) unconnected
13	XOUT	A, O	Crystal oscillator out
33	PCLK	D, O	Pixel clock output
35	OEN	D, I, N	Output enable. 0: enable, 1: disable
31	SIF ID	D, I, N	LSB of SIF slave address
32	MSSEL	D, I, U	SIF master/slave selection. 0: slave, 1: master
2	SCL	D, I/O	SIF clock
1	SDA	D, I/O	SIF data
10	POWERDN	D, I, N	Power down control, 0: power down, 1: active
17	RSET	A, I	Resistor to ground = 25 KΩ @ 48 MHz main clock, (or 50KΩ @ 24 MHz main clock)
8	RSTN	D, I, U	Chip reset, active low
48	DOUT[10]	D, I/O	Data output bit 10
47	DOUT[9]	D, I/O	Data output bit 9
46	DOUT[8]	D, I/O	Data output bit 8
45	DOUT[7]	D, O	Data output bit 7
44	DOUT[6]	D, I/O	Data output bit 6; if pulled up/down, the initial value of TIMING_CONTROL_LOW[2] (VSYNC polarity) is 1/0
43	DOUT[5]	D, I/O	Data output bit 5; if pulled up/down, the initial value of TIMING_CONTROL_LOW[1] (HSYNC polarity) is 1/0
40	DOUT[4]	D, I/O	Data output bit 4; if pulled up/down, the initial value of AD_IDL[3] (Sub ID) is 1/0
39	DOUT[3]	D, I/O	Data output bit 3; if pulled up/down, the initial value of AD_IDL[2] (Sub ID) is 1/0
38	DOUT[2]	D, I/O	Data output bit 2; if pulled up/down, the initial value of AD_IDL[1] (Sub ID) is 1/0
37	DOUT[1]	D, I/O	Data output bit 1; if pulled up/down, the initial value of AD_IDL[0] (Sub ID) is 1/0
36	DOUT[0]	D, I/O	Data output bit 0; if pulled up/down, the synchronization mode is in master/slave mode which requires HSYNC and VSYNC operating in output/input mode
3	HSYNC	D, I/O	Horizontal sync signal
5	VSYNC	D, I/O	Vertical sync signal
34	FLASH	D, O	Flash light control
15	RAMP	A, O	Analog ramp output
30,7	VDDA	P	Sensor analog power
29,9	GNDA	P	Sensor analog ground
19	VDDD	P	Sensor digital power
18	GNDD	P	Sensor digital ground
41,4	VDDK	P	Digital power

42,6	GNDK	P	Digital ground

Class Code: A – Analog signal, D – Digital signal, I – Input, O – Output, P – Power or ground, U – Internal pull-up, N – Internal pull-down

2. Functional Description

ICM-107B is a single-chip digital color imaging device. It includes a 1152x864 sensor array, 1152 column-level ADC, and correlated double sampling circuitry. All the programmable parameters are set by writing into the SIF interface which can address the register file consisting of 8-bit registers. The output format is 10-bit raw data, together with horizontal and vertical sync signals.

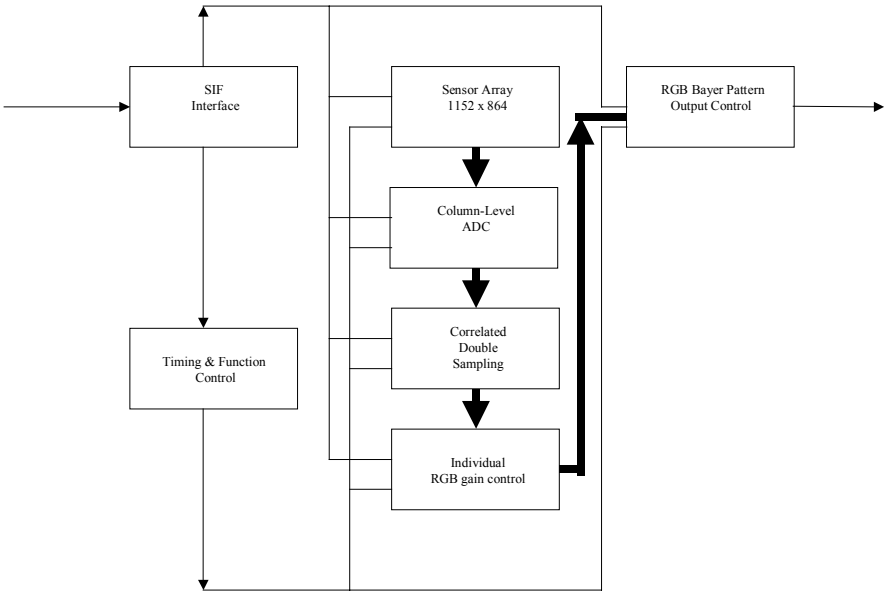


Figure 1. Block diagram

2.1 Image Array

The image array consists of 1152x864 pixels. Each pixel has a light sensitive photo diode and a set of control transistors. At the beginning of the cycle, a row of pixels is pre-charged to its maximum value. Then the row is exposed to light for several lines worth of time and sampled by the ADC. A "Correlated Double Sampling (CDS)" process is performed with subtracting the reset value (sampled right before sampling the signal) from the signal value. The purpose of CDS is to eliminate the point-wise fixed pattern noise (FPN). The output of CDS is approximately proportional to the amount of received light, ranging from 0 to 1023.

2.2 Color Filter

Each pixel is covered by a color filter. They form the Bayer Pattern as shown in Figure 2. (Row 0, Column 0) is covered by a Red filter, (Row 0, Column 1) and (Row 1, Column 0) by Green filters, and (Row 1, Column 1) by a Blue filter. Since each pixel only gets part of the frequency band, the data need further processing (i.e., color interpolation and color correction) in order to approximate the full visible spectrum.

R	**G**	R	G	R	G	R	G
G	**B**	G	B	G	B	G	B
R	G	R	G	R	G	R	G
G	B	G	B	G	B	G	B

Figure 2. Color filter Bayer pattern

2.3 Exposure and Gain Control

The brightness of the scene may change by a great amount that renders the captured image either over-exposed or under-exposed. To accommodate for different brightness, the user may change the exposure time by adjusting the AD_EXPOSE_TIMEH, and AD_EXPOSE_TIMEL. The exposure time is measured in terms of the time to read out one line of data, which is equal to 31.25 µs (assuming the line length is 1500 @ 48 MHz). If the number of lines per frame is set at 1100 (the default), the exposure time can vary from 1 to 1100 lines. In addition, users can adjust registers AD_M1_L, AD_M1_H, AD_M2_L, AD_M2_H, AD_M3_L, AD_M3_H, AD_M4_L, AD_M4_H, to optimize the individual R/G1/G2/B gain (default at 3.8 format for 1/256 to 8) of the 4 Bayer pattern pixels separately.

2.4 Timing Control

Timing control is performed with programming a 32-entry wave table. Its content can be filled by external circuitry after power up if other than default values are desirable. Bits 19 to 11 are the control signals. Bits 10 to 0 are the change position. Whenever the change position equals the column counter, a new set of signal values are applied. Please see the Wave Table Programming section for details.

2.5 Output Format

During normal operation, the output format is 10-bit raw data that ranges from 0 to 1023. It may be used for off-chip color processing or compression. A typical configuration is to connect ICM-107B to a USB1, a USB2, or a 1394/Compression combo chip. At 30 fps, the PCLK and main clock are both operating at 48 MHz.

In addition to the data pins, the chip also output VSYNC, HSYNC, and PCLK. The length and polarity of VSYNC and HSYNC can be adjusted through registers. The line and frame timing can be adjusted through registers AD_WIDTH and AD_HEIGHT.

2.6 SIF Interface

Register programming is through SIF interface (SCL and SDA pins). The default 7-bit SIF device address is 0x20, meanwhile the last bit can be configured by the SIF ID pin. ICM-107B can operate in either SIF master mode or slave mode right after power up, depending on the pull-up or pull-down of the MSSEL pin. When MSSEL is pulled low during power-up, ICM-107B's SIF interface is operated as an SIF slave device, waiting to be controlled by an external SIF master such as a microprocessor. When MSSEL is pulled high during power-up, the SIF interface is first acting as an SIF master device trying to read from an external SIF EEPROM. After that, it will fall back to behave like an SIF slave.

3. SIF Registers

Address	Name	Default	Description
0x00	PART_CONTROL	0	Processing control [0] 0: normal video mode, 1: single frame mode [1] Slope adjustment enable [2] Exposure time control, writing a 1 will activate the new value set in AD_EXPOSE_TIME, when read back from it, 0 means either the exposure time change is finished (in video mode) or the entire frame is transmitted (in single frame mode), 1 means either the exposure time change is still in progress (in video mode) or the frame is yet to finish (in single frame mode) [3] 0: normal mode, 1:sub-sampling mode [6:4] Frame rate, 0: 30 fps 1: 15 fps 2: 10 fps 3: 5 fps 4: 4 fps 5: 3 fps 6: 2 fps 7: 1 fps [7] Latent change, writing a 1 means the changed latent registers now starts taking effect, when the entire operation is done, the read back value of this bit will change from 1 to 0.
0x01 0x02	TIMING_CONTROL_LOW TIMING_CONTROL_HIGH	0x0011	Timing control [0] Column count enable, set to 0 reserved, set to 1 when normal operation [1] HSYNC polarity, 0: active low, 1: active high, the initial value is determined by DOUT[5] [2] VSYNC polarity, 0: active low, 1: active high, the initial value is determined by DOUT[6] [3] Auto dark correction enable [4] Timing select, 0: wave table timing, 1: default timing [6] Flash polarity, 0: active low, 1: active high [7] Blank polarity, 0: active low, 1: active high [8] reserved

			[10] Capture: when in single frame mode, writing a 1 here will start a frame capture [12] reserved [13] reserved
0x0C 0x0D	AD_WIDTHL AD_WIDTHH	0x05DC (1500)	[10:0] Frame width
0x0E 0x0F	AD_HEIGHTL AD_HEIGHTH	0x044C (1100)	[15:0] Frame height, should not be less than AD_ROW_BEGIN + (874)
0x10 0x11	AD_COL_BEGINL AD_COL_BEGINH	0x0064 (100)	[10:0] Beginning of active line in terms of column position [11] Mirror image enable [12] Up-down image enable
0x14 0x15	AD_ROW_BEGINL AD_ROW_BEGINH	0x000A (10)	[15:0] Beginning of active frame in terms of row position
0x18 0x19	AD_HSYNC_ENDL AD_HSYNC_ENDH	0x0040 (64)	[10:0] End of horizontal sync in terms of column position
0x1A 0x1B	AD_VSYNC_ENDL AD_VSYNC_ENDH	0x0003 (3)	[15:0] End of vertical sync in terms of row position
0x1C 0x1D	AD_EXPOSE_TIMEL AD_EXPOSE_TIMEH	0x044B (1099)	[15:0] Exposure time in terms of number of rows
0x20 0x21	AD_M1_L AD_M1_H	0x100 (256)	[10:0] Gain coefficient (G1) , in unsigned 3.8 (default) format
0x22 0x23	AD_M2_L AD_M2_H	0x100 (256)	[10:0] Gain coefficient (R) , in unsigned 3.8 (default) format
0x24 0x25	AD_M3_L AD_M3_H	0x100 (256)	[10:0] Gain coefficient.(B) , in unsigned 3.8 (default) format
0x26 0x27	AD_M4_L AD_M4_H	0x100 (256)	[10:0] Gain coefficient.(G2) , in unsigned 3.8 (default) format
0x40 0X41	AD_DARK_DATA_L AD_DARK_DATA_H	0	[9:0] When auto dark correction is disabled, serve as the subtrahend for dark correction
0x42 0x43	AD_HighLimit	3FF (1023)	[9:0] Apply dead pixel removal algorithm only to those pixel above HighLimit
0x44 0x45	AD_LowLimit	0	[9:0] Apply dead pixel removal algorithm only to those pixel below LowLimit
0x52	AD_INOUTSEL	0	[4:0] Output format 0: default, unsigned 3.8 format 1: default, unsigned 4.7 format 2: default, unsigned 5.6 format 3: default, unsigned 6.5 format 0-7: 10-bit raw data 8: reserved 9: reserved 10: reserved 11: dead pixel removal algorithm enable 12: reserved 13: sub-sampling data output (1/4 format) 14-31: reserved

0x53	AD_RAMPSEL	0	[7] reserved
0x54 0x55	AD_DSRSTL AD_DSRSTH	0x0000 (0)	[10:0] reserved
0x56 0x57	AD_DSDATAL AD_DSDATAH	0x07D0 (2000)	[10:0] reserved
0x82 0x83	AD_IDL AD_IDH	0x1070 (4208)	[3:0] Sub ID, Read from pins DOUT[4:1] during reset [15:4] Device ID, default 0x107 , can be configured using SIF
0x84 0x85	AD_FLASH_BEGINL AD_FLASH_BEGINH	0x036A (874)	[15:0] Flash light begin position in terms of rows
0x86 0x87	AD_FLASH_ENDL AD_FLASH_ENDH	0x037E (894)	[15:0] Flash light end position in terms of rows
0x88 0x89	AD_BWIDTH_BEGINL AD_BWIDTH_BEGINH	0x0068 (104)	[10:0] Blank begin in terms of columns
0x8A 0x8B	AD_BWIDTH_ENDL AD_BWIDTH_ENDH	0x04E7 (1255)	[10:0] Blank end in terms of columns/ need [10:0]
0x8C 0x8D	AD_BHEIGHT_BEGINL AD_BHEIGHT_BEGINH	0x000E (14)	[15:0] Blank begin in terms of rows
0x8E 0x8F	AD_BHEIGHT_ENDL AD_BHEIGHT_ENDH	0x036D (877)	[15:0] Blank end in terms of rows
0x90	AD_RSTSEL	0x40	[7:6] RSTL voltage select 0: 0.7 V 1: 0.9 V (default) 2: 1.1 V
0x94	AD_BITCONTROL	C0	reserved
0x97 0x98	AD_WT_BEGINL AD_WT_BEGINH	0	reserved
0x99 0x9A	AD_WT_ENDL AD_WT_ENDH	0x07F8 (2040)	Reserved
0x9B 0x9C	AD_SUB_EN_TIMEL AD_SUB_EN_TIMEH	0x05BE (1470)	Reserved
0xA1 0xA2	AD_WIDTHL_C AD_WIDTHH_C	0x05DC (1500)	[10:0] Current frame width, read only
0xA3 0xA4	AD_HEIGHTL_C AD_HEIGHTH_C	0x044C (1100)	[15:0] Current frame height, read only
0xA5 0xA6	AD_COL_BEGINL_C AD_COL_BEGINH_C	0x0064 (100)	[10:0] Current column beginning position, read only
0xA7 0xA8	AD_ROW_BEGINL_C AD_ROW_BEGINH_C	0x000A (10)	[10:0] Current row beginning position, read only
0xA9 0xAA	AD_HSYNC_ENDL_C AD_HSYNC_ENDH_C	0x0040 (64)	[10:0] Current HSync end position, read only
0xAB 0xAC	AD_VSYNC_ENDL_C AD_VSYNC_ENDH_C	0x0003 (3)	[15:0] Current VSync end position, read only
0xAD	AD_PART_CONTROL_C	0x00 (0)	[7:0] Current part control setting, read only
0xAE 0xAF	AD_WT_BEGINL_C AD_WT_BEGINH_C	0	[10:0] Current wave table beginning point, read only

0xB0 0xB1	AD_WT_ENDL_C AD_WT_ENDH_C	0x07F8 (2040)	[10:0] Current wave table end point, read only
0xB4	AD_PLL	0x07	[4:0] PLL setting for ADC clock. For example, at 6 MHz input, selection of [00011] will run system ADC clock at 24MHz. Note: maximum ADC clock is 96MHz for 30 fps operation. 00000: x1 for PLL 00001: x2 for PLL 00011: x4 for PLL 00111: x8 for PLL 01111: x16 for PLL
0xB6 0xB7	AD_F_MAX_ADDRL AD_F_MAX_ADDRH	369(873)	Reserved for debugging purpose
0xB8 0xB9	AD_F_OVERL AD_F_OVERH	36A(874)	Reserved for debugging purpose
0xBA 0xBB	AD_F_LIMITAL AD_F_LIMITAH	36B(875)	Reserved for debugging purpose
0xBC 0xBD	AD_F_LIMITBL AD_F_LIMITBH	2(2)	Reserved for debugging purpose
0xBE 0xBF	AD_F_LIMITCL AD_F_LIMITCH	36A(874)	Reserved for debugging purpose
0xC0 0xC1 0xC2 0xC3	AD_COL_DEAD0L AD_COL_DEAD0H AD_ROW_DEAD0L AD_ROW_DEAD0H	07FF 07FF	Dead pixel #0 address A total of 12 pixels
0xC4 0xC5 0xC6 0xC7	AD_COL_DEAD0L AD_COL_DEAD0H AD_ROW_DEAD0L AD_ROW_DEAD0H	07FF 07FF	Dead pixel #1 address
0xC8 0xC9 0xCA 0xCB	AD_COL_DEAD0L AD_COL_DEAD0H AD_ROW_DEAD0L AD_ROW_DEAD0H	07FF 07FF	Dead pixel #2 address
0xCC 0xCD 0xCE 0xCF	AD_COL_DEAD0L AD_COL_DEAD0H AD_ROW_DEAD0L AD_ROW_DEAD0H	07FF 07FF	Dead pixel #3 address
0xD0 0xD1 0xD2 0xD3	AD_COL_DEAD0L AD_COL_DEAD0H AD_ROW_DEAD0L AD_ROW_DEAD0H	07FF 07FF	Dead pixel #4 address
0xD4 0xD5 0xD6 0xD7	AD_COL_DEAD0L AD_COL_DEAD0H AD_ROW_DEAD0L AD_ROW_DEAD0H	07FF 07FF	Dead pixel #5 address
0xD8 0xD9	AD_COL_DEAD0L AD_COL_DEAD0H	07FF 07FF	Dead pixel #6 address

0xDA 0xDB	AD_ROW_DEAD0L AD_ROW_DEAD0H		
0xDC 0xDD 0xDE 0xDF	AD_COL_DEAD0L AD_COL_DEAD0H AD_ROW_DEAD0L AD_ROW_DEAD0H	07FF 07FF	Dead pixel #7 address
0xE0 0xE1 0xE2 0xE3	AD_COL_DEAD0L AD_COL_DEAD0H AD_ROW_DEAD0L AD_ROW_DEAD0H	07FF 07FF	Dead pixel #8 address
0xE4 0xE5 0xE6 0xE7	AD_COL_DEAD0L AD_COL_DEAD0H AD_ROW_DEAD0L AD_ROW_DEAD0H	07FF 07FF	Dead pixel #9 address
0xE8 0xE9 0xEA 0xEB	AD_COL_DEAD0L AD_COL_DEAD0H AD_ROW_DEAD0L AD_ROW_DEAD0H	07FF 07FF	Dead pixel #10 address
0xEC 0xED 0xEE 0xEF	AD_COL_DEAD0L AD_COL_DEAD0H AD_ROW_DEAD0L AD_ROW_DEAD0H	07FF 07FF	Dead pixel #11 address

4. Electrical Characteristics

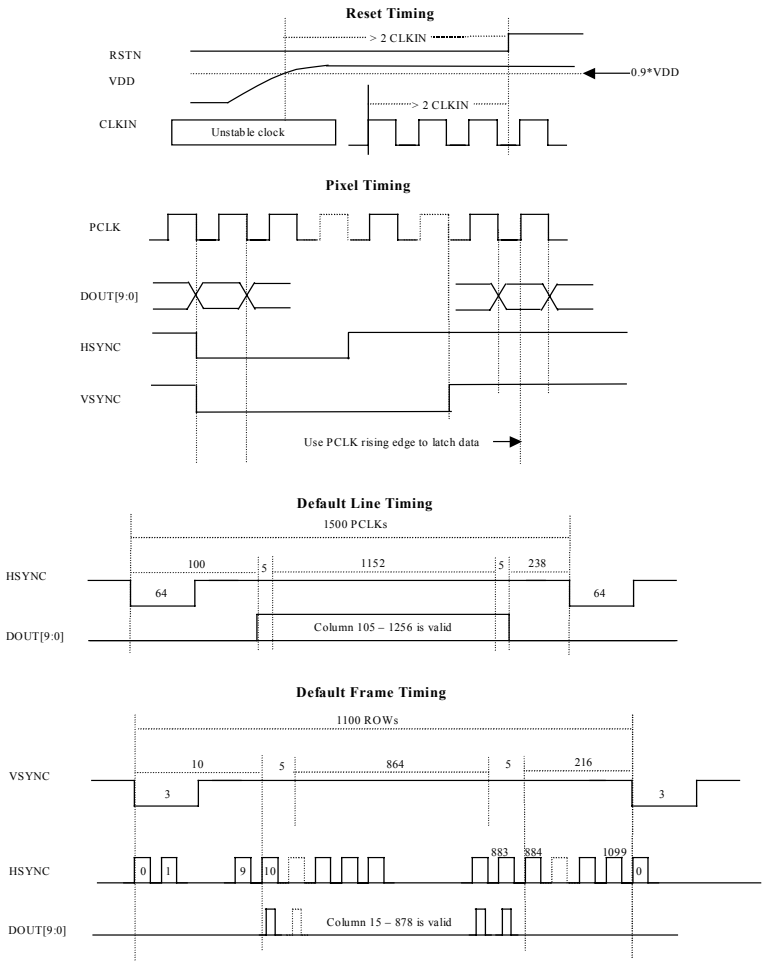
4.1 DC Characteristics

Symbol	Parameter	Rating			Unit
		Minimum	Typical	Maximum	
V_{CCA}	Absolute Power Supply	-0.3		3.8	V
V_{INA}	Absolute Input Voltage	-0.3		V_{CC} + 0.3	V
V_{OUTA}	Absolute Output Voltage	-0.3		V_{CC} + 0.3	V
T_{STG}	Storage Temperature	0	25	65	°C
V_{CC} Digital (V_{CC} Analog)	Operating Power Supply	3.0	3.3	3.6	V
V_{IN}	Operating Input Voltage	0		V_{CC}	V
T_{OPR}	Operating Temperature	0	25	55	°C
I_{DD}	Operating Current @ V_{CC}=3.3 V, 25 °C		100		mA
I_{IL}	Input Low Current	-1		1	µA
I_{IH}	Input High Current	-1		1	µA
I_{OZ}	Tri-state Leakage Current	-10		10	µA
C_{IN}	Input Capacitance		3		pF
C_{OUT}	Output Capacitance		3		pF

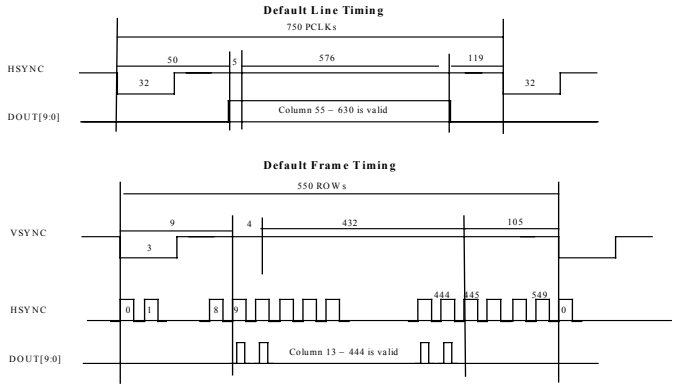
C_{BID}	Bi-directional Buffer Capacitance		3		pF
V_{IL}	Input Low Voltage			0.3 * V_{CC}	V
V_{ILS}	Schmitt Input Low Voltage		1.1		V
V_{IH}	Input High Voltage	0.7 * V_{CC}			V
V_{IHS}	Schmitt Input High Voltage		1.8		V
V_{OL}	Output Low Voltage			0.4	V
V_{OH}	Output High Voltage	2.4			V
R_L	Input Pull-up/down Resistance		50		KΩ

4.2 Timing

4.2.1 MegaPixel Mode



5.2.2 Sub-sampling Quarter Mega Pixel Mode



5.3 Pixel Clock Duty Cycle

In different frame rate mode (controlled by PART_CONTROL [6:4]), the duty cycle (high time / clock period) of the PCLK signal is described in the following table:

Frame Rate	Duty Cycle
30	50.0%
15	50.0%
10	50.0%
5	50.0%
4	53.3%
3	50.0%
2	50.0%
1	50.0%

5 Mechanical Information

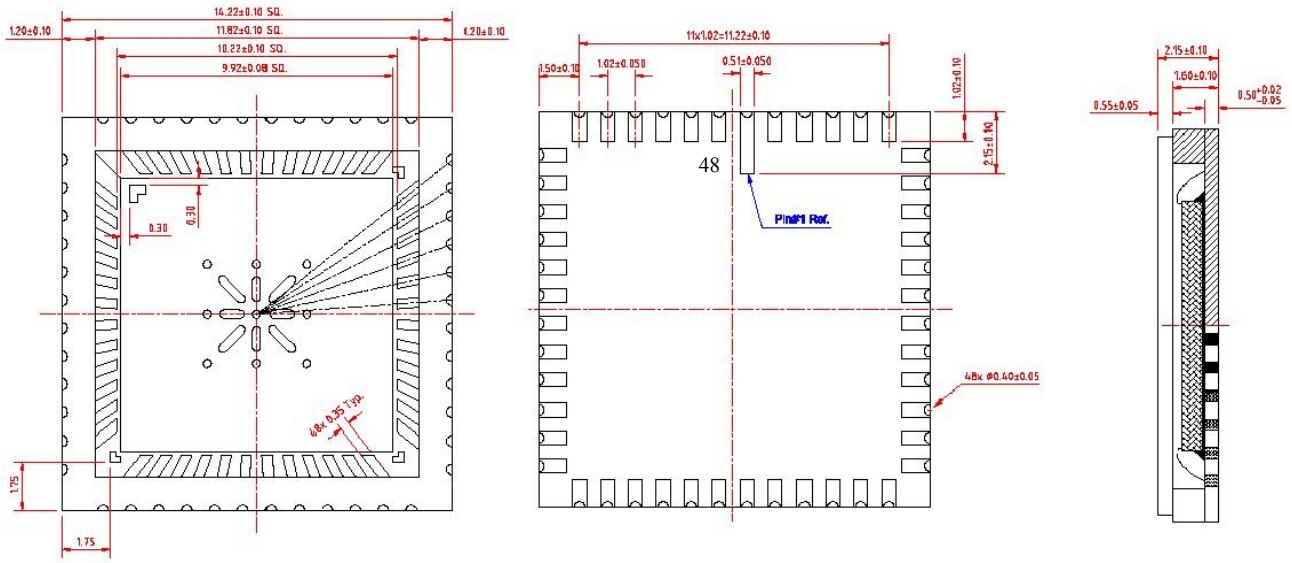


Figure 3. Plastic LCC48 Packaging

6 Ordering Information

Description	*Part Number*
Plastic LCC 48 packaged, MegaPixel resolution sensor (3.3 V)	ICM-107Bpa

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