CATALYST

CAT24C21

1-kb Dual Mode Serial EEPROM for VESA™ "Plug-and-Play"

HALOGEN FREE
LEAD FREE ™

FEATURES

- DDC1™/DDC2™ interface compliant for monitor identification
- 400 kHz I²C bus compatible*
- 2.5 to 5.5 volt operation
- 16-byte page write buffer
- Hardware write protect

- Low power CMOS technology
- 1,000,000 program/erase cycles
- 100 year data retention
- 8-pin DIP, SOIC, TSSOP, MSOP or TDFN packages
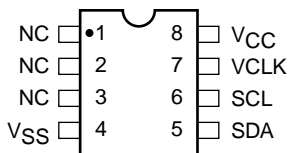- Industrial temperature range

DESCRIPTION

The CAT24C21 is a 1-kb Serial CMOS EEPROM internally organized as 128 words of 8 bits each. The device complies with the Video Electronics Standard Association's (VESA™), Display Data Channel (DDC™) standards for "Plug-and-Play" monitors. The "transmit-only" mode (DDC1™) is controlled by the VCLK clock 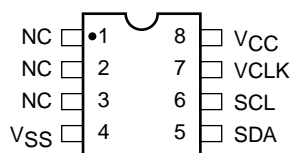input and the "bi-directional" mode (DDC2™) is controlled by the SCL clock input, with both modes sharing a common SDA input/output (I/O). The transmit-only mode is a read-only mode, while the bi-directional mode is a read and write mode following the I²C protocol. In write mode the CAT24C21 features a 16-byte page write buffer. The device is available in 8-in DIP, SOIC, TSSOP, MSOP and TDFN packages.
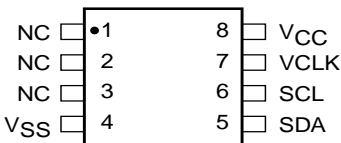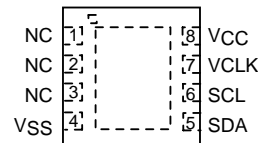
PIN CONFIGURATION

DIP Package (P, L)

NC	•1	8	V$_{CC}$
NC	2	7	VCLK
NC	3	6	SCL
V$_{SS}$	4	5	SDA

SOIC Package (J, W)

NC	•1	8	V$_{CC}$
NC	2	7	VCLK
NC	3	6	SCL
V$_{SS}$	4	5	SDA

MSOP Package (R, Z)

NC	•1	8	V$_{CC}$
NC	2	7	VCLK
NC	3	6	SCL
V$_{SS}$	4	5	SDA

TDFN Package (RD4, ZD4)

NC	1	8	V$_{CC}$
NC	2	7	VCLK
NC	3	6	SCL
V$_{SS}$	4	5	SDA

3 mm x 3 mm
Top View

TSSOP Package (U, Y)

NC	•1	8	V$_{CC}$
NC	2	7	VCLK
NC	3	6	SCL
V$_{SS}$	4	5	SDA

* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

FUNCTIONAL SYMBOL

V$_{CC}$

SCL → [CAT24C21] ↔ SDA

VCLK →

V$_{SS}$
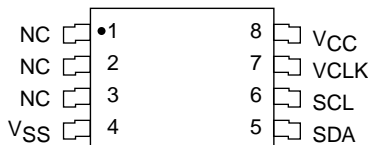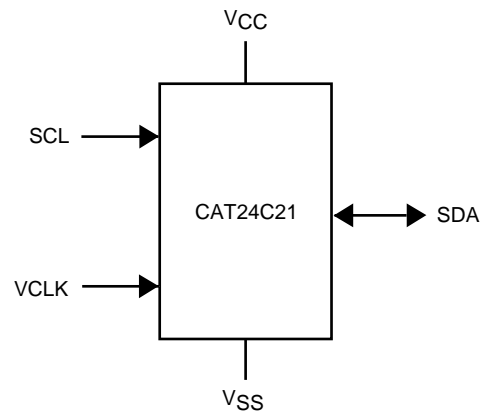
PIN FUNCTIONS

Pin Name	Function
NC	No Connect
SDA	Serial Data/Address
SCL	Serial Clock (bi-directional mode)
VCLK	Serial Clock (transmit-only mode)
V$_{CC}$	Power Supply
V$_{SS}$	Ground

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... -55°C to +125°C

Storage Temperature .... -65°C to +150°C

Voltage on Any Pin with
Respect to Ground[1] .... -2.0 V to V_{CC} + 2.0 V

V_{CC} with Respect to Ground .... -2.0 V to +7.0 V

Package Power Dissipation
Capability (T_A = 25°C) .... 1.0 W

Lead Soldering Temperature (10 seconds) ...... 300°C

Output Short Circuit Current[2] .... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Reference Test Method	Min	Units
N_{END}[3][*]	Endurance	MIL-STD-883, Test Method 1033	1,000,000	Program/Erase Cycles
T_{DR}[3]	Data Retention	MIL-STD-883, Test Method 1008	100	Years
V_{ZAP}[3]	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000	Volts
I_{LTH}[3][4]	Latch-up	JEDEC Standard 17	100	mA

(*) Page Mode, V_{CC} = 5 V, 25°C

D.C. OPERATING CHARACTERISTICS

V_{CC} = 2.5 V to 5.5 V, unless otherwise specified. Industrial temperature range.

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CC}	Power Supply Current	f_{SCL} = 400 kHz		2	mA
I_{SB}[5]	Standby Current	V_{IN} = GND or V_{CC}		1	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		10	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		10	µA
V_{IL}	Input Low Voltage		−1	V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	V_{CC} = 3.0 V, I_{OL} = 3 mA		0.4	V
V_{IL}	Input Low Voltage (VCLK)	V_{CC} ≥ 2.7 V		0.8	V
V_{IH}	Input High Voltage (VCLK)		2.0		V

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5 V

Symbol	Parameter	Conditions	Min	Max	Units
$C_{I/O}$[3]	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0 V		8	pF
C_{IN}[3]	Input Capacitance (VCLK, SCL)	V_{IN} = 0 V		6	pF

Note:
(1) The minimum DC input voltage is −0.5 V. During transitions, inputs may undershoot to −2.0 V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods of less than 20 ns.
(2) Output shorted for no more than one second.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on I/O pins from −1 V to V_{CC} + 1 V.
(5) Maximum standby current (I_{SB}) = 10µA for the Extended Automotive temperature range.

A.C. CHARACTERISTICS

V_{CC} = 2.5 V to 5.5 V, unless otherwise specified. Industrial temperature range.

Symbol	Parameter	Min	Max	Units
Transmit-only Mode				
T_{VAA}	Output valid from VCLK		0.5	µs
T_{VHIGH}	VCLK high	0.6		µs
T_{VLOW}	VCLK low	1.3		µs
T_{VHZ}	Mode transition		0.5	µs
T_{VPU}	Transmit-only power-up	0		ns
Read & Write Cycle Limits				
F_{SCL}	Clock Frequency		400	kHz
$T_I{}^{(1)}$	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		1	µs
$t_{BUF}{}^{(1)}$	Time the Bus Must be Free Before a New Transmission Can Start	1.2		µs
$t_{HD:STA}$	Start Condition Hold Time	0.6		µs
t_{LOW}	Clock Low Period	1.2		µs
t_{HIGH}	Clock High Period	0.6		µs
$t_{SU:STA}$	Start Condition Setup Time	0.6		µs
$t_{HD:DAT}$	Data In Hold Time	0		ns
$t_{SU:DAT}$	Data In Setup Time	50		ns
$t_R{}^{(1)}$	SDA and SCL Rise Time		0.3	µs
$t_F{}^{(1)}$	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	0.6		µs
t_{DH}	Data Out Hold Time	100		ns
Power-Up Timing[(1)(2)]				
t_{PUR}	Power-up to Read Operation		1	ms
t_{PUW}	Power-up to Write Operation		1	ms
Write Cycle Limits				
t_{WR}	Write Cycle Time		5	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

PIN DESCRIPTION

The SCL serial clock input pin is used to clock all data transfers into or out of the device when in the bi-directional mode.

The SDA bi-directional serial data/address pin is used to transfer data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

FUNCTIONAL DESCRIPTION

The CAT24C21 has two modes of operation: the transmit-only mode and the bi-directional mode. There is a separate 2-wire protocol to support each mode, each having a separate clock input (VCLK and SCL respectively) and both modes sharing a common bi-directional data line (SDA). The CAT24C21 enters the transmit-only mode upon power up and begins outputting data on the SDA pin with each clock signal on the VCLK pin. The device will remain in the transmit-only mode until there is a valid HIGH to LOW transition on the SCL pin, when it will switch to the bi-directional mode (Figure 1). Once in the bi-directinal mode, the only way to return to the transmit-only mode is by powering down the device.

The VCLK serial clock input pin is used to clock data out of the device when in transmit-only mode. When held low, in bi-directional mode, it will inhibit write operations.

TRANSMIT-ONLY MODE: (DDC1)

Upon power-up, the CAT24C21 will output valid data only after it has been initialized. During initialization, data will not be available until after the first nine clocks are sent to the device (Figure 2). The starting address for the transmit-only mode can be determined during initialization. If the SDA pin is high during the first eight clocks, the starting address will be 7FH. If the SDA pin is low during the first eight clocks, the starting address will be 00H. During the ninth clock, SDA will be in the high impedance state.

Data is transmitted in 8 bit words with the most significant bit first, followed by a 9th 'don't care' bit which will be in the high impedance state (Figure 3). The CAT24C21 will continuously sequence through the entire memory array as long as VCLK is present and no falling edges on SCL are detected. When the maximum address (7FH) is reached, addressing will wrap around to the zero location (00H) and transmitting will continue. The bi-directional mode clock (SCL) pin must be held high for the device to remain in the transmit-only mode.
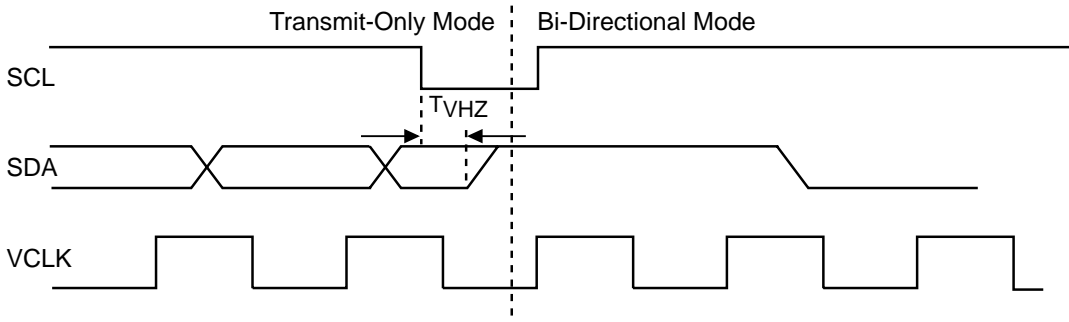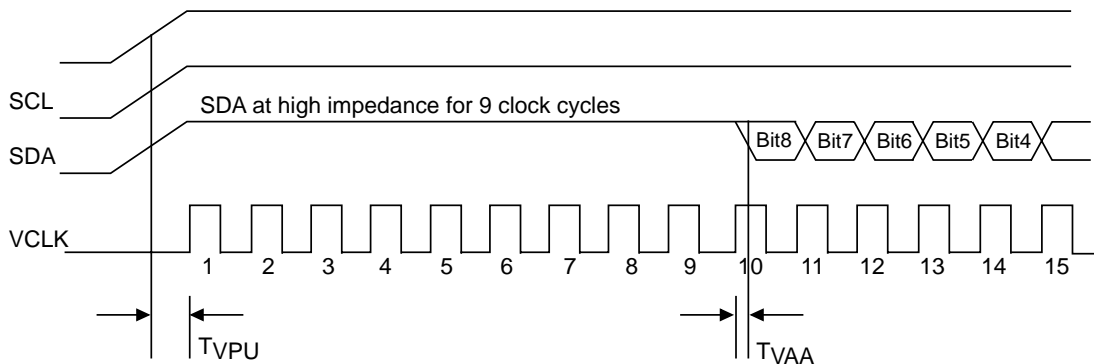
Figure 1. Mode Transition

Figure 2. Device Initialization for Transmit-only Mode

BI-DIRECTIONAL MODE (DDC2)

The following defines the features of the I²C bus protocol in bi-directional mode (Figure 4):

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

When in the bi-directional mode, all inputs to the VCLK pin are ignored, except when a logic high is required to enable write capability.

START Condition

The START condition (Figure 6) precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24C21 monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

Device Addressing

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are fixed as 1010 for the CAT24C21 (see Fig. 8). The next three significant bits are "don't care". The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master sends a START condition and the slave address byte, the CAT24C21 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24C21 then performs a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

Figure 3. Transmit-only Mode
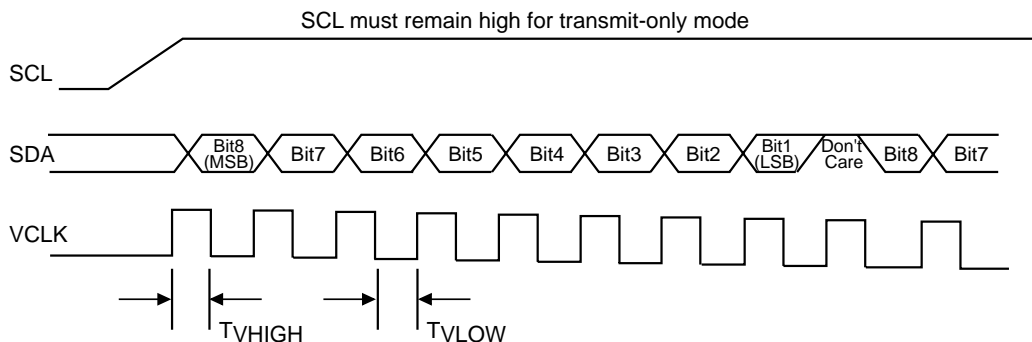
Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge (ACK). The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it has received the 8 bits of data (Figure 7).

The CAT24C21 responds with an ACK after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an ACK after receiving each 8-bit byte.

When the CAT24C21 is in a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an ACK. Once it receives this ACK, the CAT24C21 will continue to transmit data. If no ACK is sent by the Master, the device terminates data transmission and waits for a STOP condition.

Write Operations

VCLK must be held high in order to program the device. This applies to byte write and page write operation. Once the device is in its self-timed program cycle, VCLK can go low and not affect programming.

Byte Write

In the Byte Write mode (Figure 9), the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an ACK, the Master sends the byte address that is to be written into the address pointer of the CAT24C21. After receiving another ACK from the Slave, the Master device transmits the data byte to be written into the addressed memory location. The CAT24C21 acknowledges once more and the Master generates the STOP condition, at which time the device begins its internal programming cycle to nonvolatile memory (Figure 5). While this internal cycle is in progress, the device will not respond to any request from the Master device.
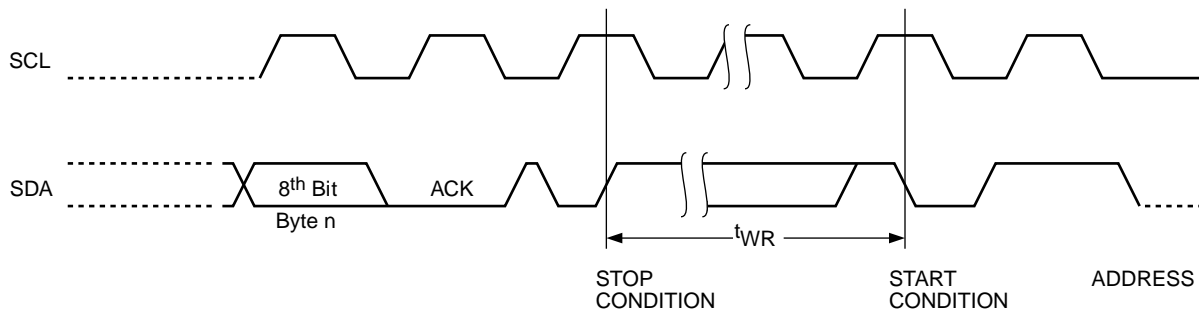
Figure 4. Bus Timing
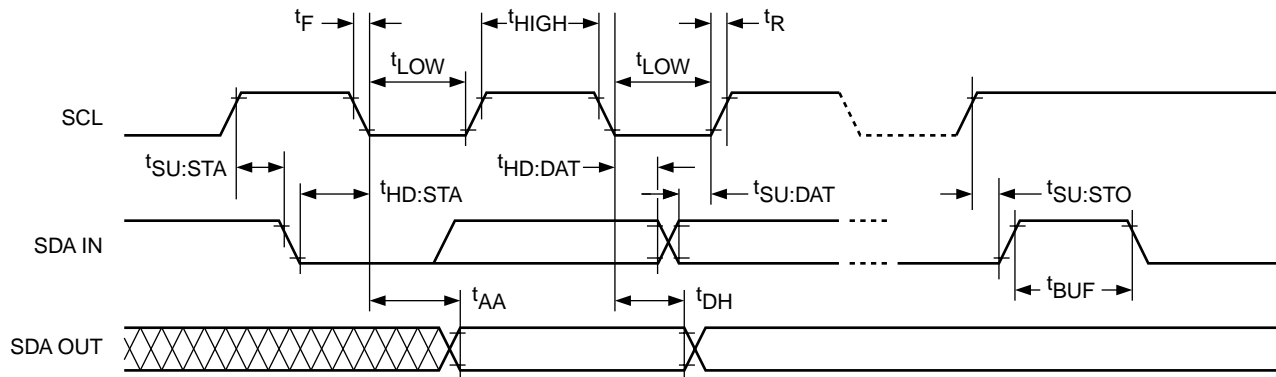
Figure 5. Write Cycle Timing

Page Write

The CAT24C21 writes up to 16 bytes of data in a single write cycle, using the Page Write operation. The Page Write operation (Figure 10) is initiated in the same manner as the Byte Write operation, however instead of terminating after the initial word is transmitted, the Master is allowed to send up to fifteen additional bytes. After each byte has been transmitted the CAT24C21 will respond with an ACK, and internally increment the low order address bits by one. The high order bits remain unchanged.

If the Master transmits more than sixteen bytes prior to sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

Once all sixteen bytes are received and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point all received data is written to the CAT24C21 in a single write cycle.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT24C21 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24C21 is still busy with the write operation, no ACK will be returned. If the CAT24C21 has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Figure 6. Start/Stop Timing
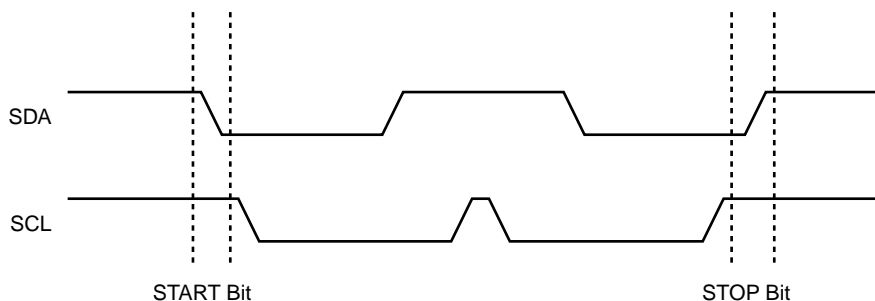
Figure 7. Acknowledge Timing
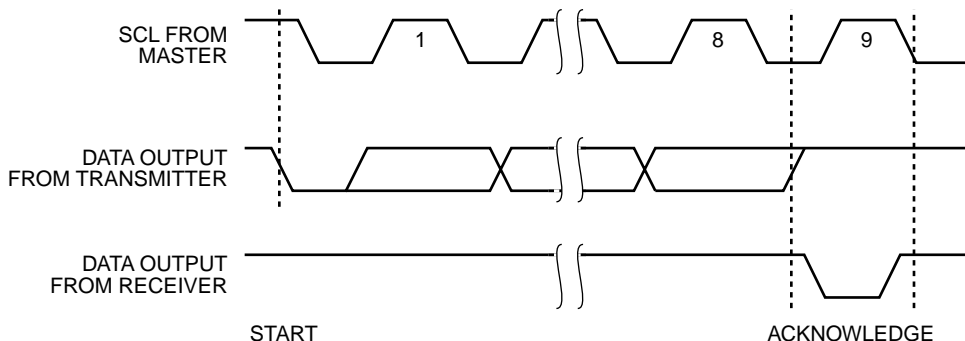
Figure 8. Slave Address Bits

1	0	1	0	X	X	X	R/$\overline{W}$

Write Protection

When the VCLK pin is connected to GND and the CAT24C21 is in the bi-directional mode, the entire memory is protected and becomes "read only".

Read Operations

The READ operation for the CAT24C21 is initiated in the same manner as the write operation with the one exception that the R/$\overline{W}$ bit is set to a one. Three different READ operations are possible: Immediate Address READ, Selective READ and Sequential READ.

Immediate Address Read

The CAT24C21's address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N + 1 (Figure 11). If N = 127, then the counter will 'wrap around' to address 0 and continue to clock out data.

Selective Read

Selective READ operations allow the Master device to select at random any memory location for a READ operation (Figure 12). The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAT24C21 acknowledges the word address, the Master device resends the START condition and the slave address, this time with the R/$\overline{W}$ bit set to one. The CAT24C21 then responds with its ACK and sends the 8-bit byte requested. The master device does not send an ACK but will generate a STOP condition.

Sequential Read

The Sequential READ operation (Figure 13) can be initiated by either the Immediate Address READ or the Selective READ operation. After the CAT24C21 sends the first 8-bit byte, the Master responds with an ACK, which tells the Slave that more data is being requested. The CAT24C21 will continue to output an 8-bit byte for each ACK sent by the Master. The entire memory content can thus be read out sequentially. If the end of memory is reached in the process, then addressing will 'wrap-around' to the beginning of memory. Data output will stop when the Master fails to acknowledge and sends a STOP condition.
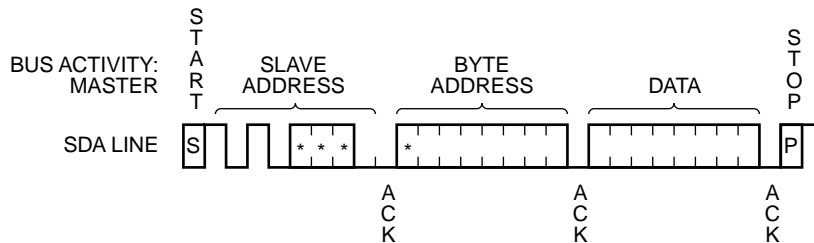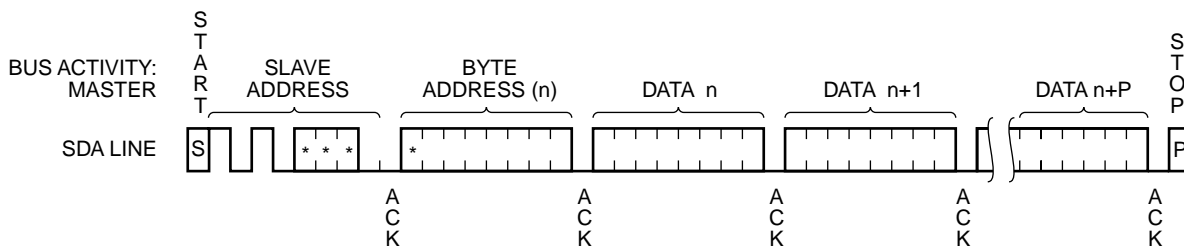
Figure 9. Byte Write Timing

Figure 10. Page Write Timing

n_{MAX} = 7FH
P = 15 for CAT24WC21
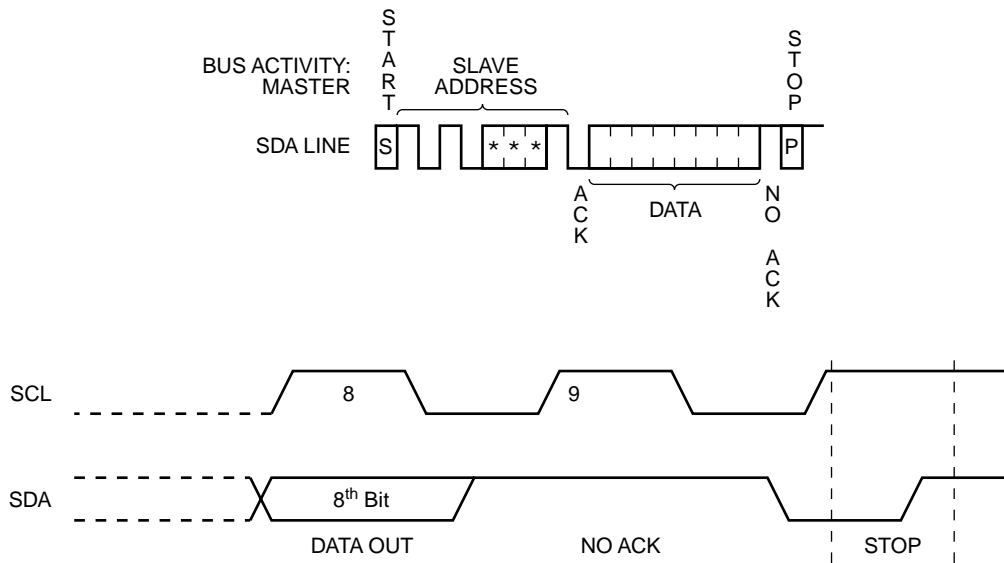* = Don't care

Figure 11. Immediate Address Read Timing
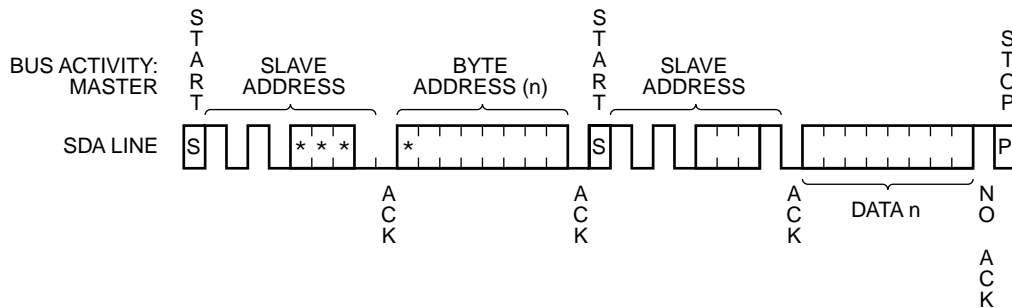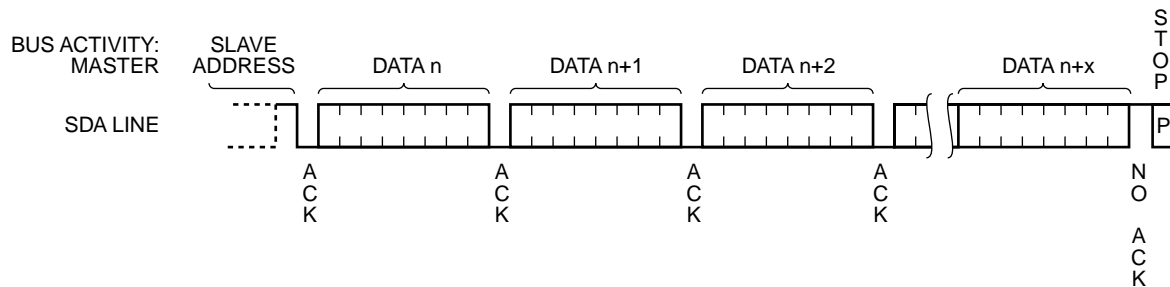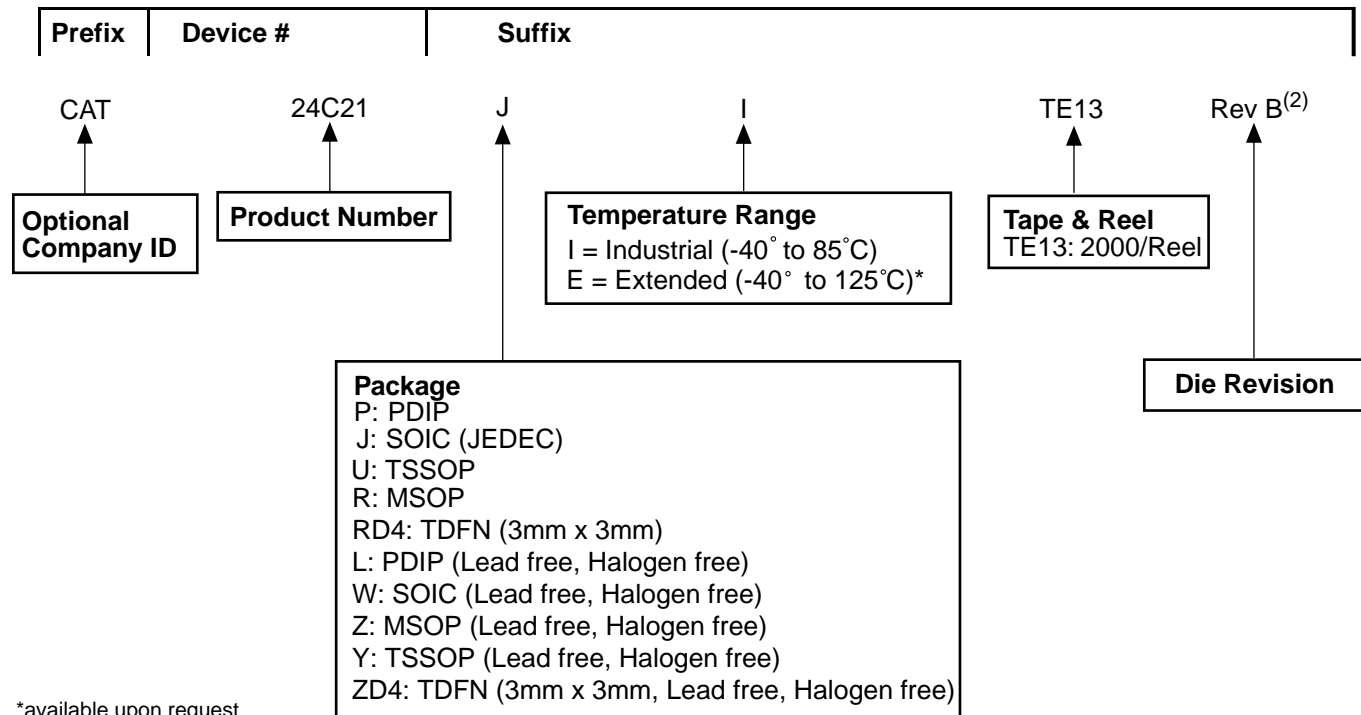

Figure 12. Selective Read Timing

Figure 13. Sequential Read Timing

ORDERING INFORMATION

Prefix	Device #	Suffix

CAT   24C21   J   I   TE13   Rev B[2]

Optional Company ID

Product Number

Temperature Range
I = Industrial (-40˚ to 85˚C)
E = Extended (-40˚ to 125˚C)*

Tape & Reel
TE13: 2000/Reel

Die Revision

Package
P: PDIP
J: SOIC (JEDEC)
U: TSSOP
R: MSOP
RD4: TDFN (3mm x 3mm)
L: PDIP (Lead free, Halogen free)
W: SOIC (Lead free, Halogen free)
Z: MSOP (Lead free, Halogen free)
Y: TSSOP (Lead free, Halogen free)
ZD4: TDFN (3mm x 3mm, Lead free, Halogen free)

*available upon request

Notes:
(1) The device used in the above example is a CAT24C21JI-TE13 (SOIC, Industrial Temperature, 2.5 Volt to 5.5 Volt Operating Voltage, Tape & Reel)
(2) Product die revision letter is marked on top of the package as a suffix to the production date code (e.g., AYWWB). For additional information, please contact your Catalyst sales office.

REVISION HISTORY

Date	Rev.	Reason
9/29/2003	H	Replaced Block Diagram with Functional Symbol Eliminated commercial temperature range Updated marking
10/15/2003	I	Added TDFN package Updated Pin Descriptions Updated DC Operating Characteristics Updated AC Characteristics Updated Byte Write Timing Figure Updated Page Write Timing Figure Updated Immediate Address Read Timing Figure
10/22/2003	J	Updated Reliability Characteristics Updated D.C. Operating Characteristics Updated Capacitance
10/24/2003	K	Formatting Change
11/12/2003	L	Corrected DC Operating Characteristics Corrected AC Characteristics
12/23/2003	M	Changed Industrial temp range from "Blank" to "I" in Ordering Information
7/7/2004	N	Added die revision to Ordering Information
7/27/2004	O	Updated DC Operating Characteristics table and notes