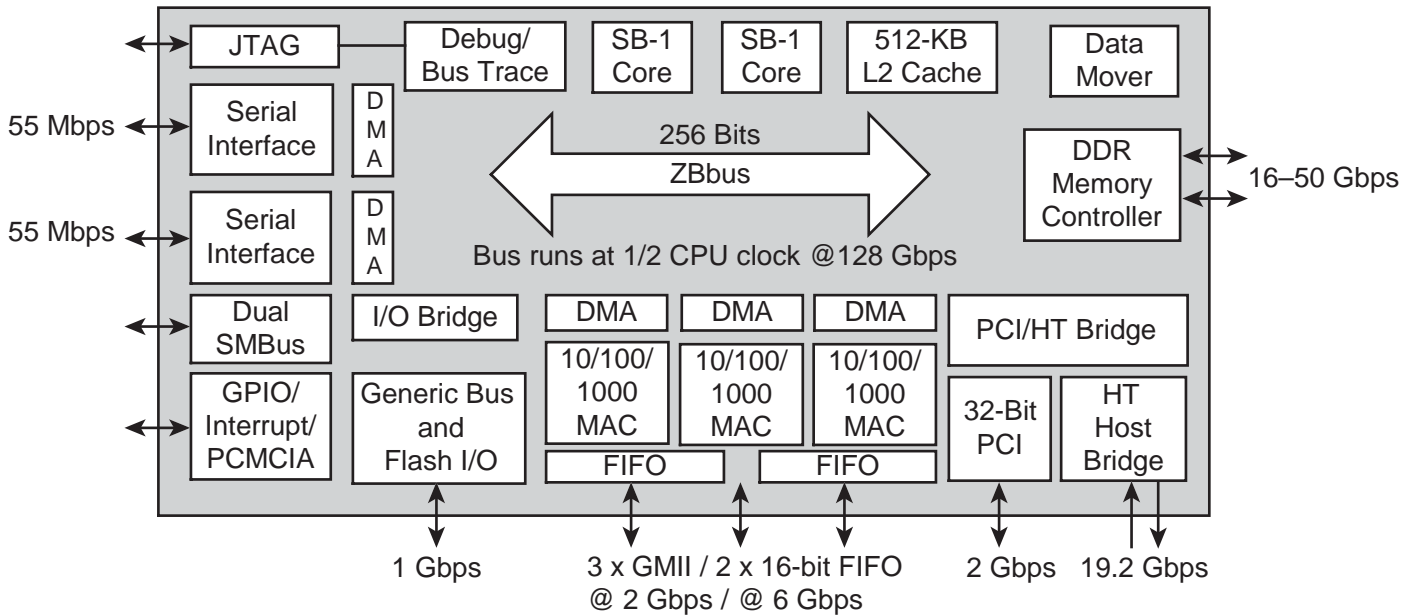


BCM1250 Block Diagram



Broadcom’s first SiByte™ processor, the **BCM1250**, is a state-of-the-art multiprocessor solution targeted at the fast-growing networking and communications markets.

The **BCM1250** is the first MIPS64™ processor to offer the industry-leading performance, high functional integration, and low power levels required by next-generation networking applications.

The **BCM1250** is an intelligent on-chip multiprocessor system (CMP) consisting of two Broadcom SB-1 high performance MIPS64™ CPUs, a shared 512-KB L2 cache, a DDR memory controller, and integrated I/O. All major blocks of the processor are connected together via the ZBbus, a high-speed, split-transaction multiprocessor bus. The bus implements the standard MESI protocol to ensure coherency between the two CPUs, L2 cache, I/O agents, and memory. Three Gigabit Ethernet MACs (10/100/1000) enable easy interfacing to LANs. To enable higher data rates, or in cases where Ethernet protocol processing is not required, the MACs can be configured as either three 8-bit or two 16-bit packet FIFOs. The high-speed I/O is provided using

HyperTransport™ (HT) I/O fabric and a 32-bit PCI (rev 2.2) local bus. Two serial ports are available to use as UARTs for console ports or asynchronous interface for WAN connections at up to T3/OC-1 rates (55 Mbps).

To enable low chip-count systems, the **BCM1250** also includes a configurable generic bus that allows glueless connection of a boot ROM or flash memory and simple I/O peripherals. On-chip debug, trace, and performance monitoring functions assist both hardware and software designers in debugging and tuning the system. The system can be run in either big- or little-endian mode. The **BCM1250** is manufactured in TSMC's 0.13µ process and is available in an 860 BGA package.

Implementation of MIPS64™ ISA

The SB-1 CPU core is a high-performance implementation of the standard MIPS64™ instruction set architecture (ISA), and incorporates the MIPS-3D and MIPS-MDMX application specific extensions (ASEs). The core supports a four-issue enhanced skew pipeline and can dispatch up to two memory and two ALU (Integer, Floating Point, MDMX or MIPS-3D) instructions per cycle.

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